

USB Based Dual T3/E3 Interfaces for WAN and Mux/Demux Testing

Structured (Channelized), Unstructured, and Unframed

T3/E3 Data Capture into File & Playback from File

ATM, HDLC, Frame-Relay and PPP Protocol Analysis

Test Mux/Demux along with Dual port T1/E1 Drop/Insert

T3/E3 Link Emulation with Error and Alarm Insertion

T3 and T3/T1 FEAC Loop Commands

Propagation Delay Emulation and Measurement

T3 and T3/T1 FEAC Loop Commands

Propagation Delay Emulation and Measurement

Dual BERT and G.821 Analysis

Tx Clock option – Internal, Recovered or External

Laptop T3 / E3 Analyzer



GL's T3/E3 Analyzers plug into USB port of PCs and provide dual T3/E3 interfaces for analyzing, testing, simulating, and monitoring T3 signals. A single T1/E1 input and output is provided to insert and receive T1 (or E1) signals into the T3/E3 stream.

The T3/E3 analyzer unit used in conjunction with GL's LaptopT1/E1 analyzer provides a complete T3/E3 (44.736 Mbps / 34.368 Mbps), T1/E1 (1.544 Mbps / 2.048Mbps), and DS0 (64Kbps) testing solutions.

Main features

- Software Selectable T3 and E3 interface along with T1 and E1 Drop and Insert
- Plug and Play to PC Interface through USB 2.0
- Manage the Analyzer remotely via Ethernet port (future)
- Dual T3/E3 Receivers and Transmitters for Non-intrusive and Intrusive testing
- Record / Playback T3/E3 Signals (Channelized, Unchannelized or Unframed) up to Hard-disk Capacity
- Channelized (Structured) Testing
 - Multiplex / De-multiplex testing
 - Receivers for bidirectional monitoring with Dual T1 / E1 drop
 - Transmit multiplexed externally inserted or internally generated T1/E1 streams into T3/E3
 - Drop User selected T1/ E1 from incoming T3/E3
 - Broadcast or Loopback Individual T1s/E1s received from T3/E3
 - Generates 28 T1s or (21 E1s) signals within the T3 (or 16 E1s within E3) output
- Unchannelized (Unstructured)
 - WAN Testing
 - ATM, Frame Relay, PPP, HDLC Protocol Analysis
 - Transmit /Verify HDLC frames with user defined headers
- General Testing
 - Dual BERT and G.821 Analysis
 - Error Injection and Alarm Generation
 - Decode and Simulate Far End Alarm Channel (FEAC) and Terminal Path Maintenance Data Link (MDL) Messages
 - Propagation Delay Emulation and Measurements
 - T3/E3 errors counters
 - Alarms – Monitoring and Logging

For more details, please visit our web page <http://www.gl.com/laptopt3e3.html>



GL Communications Inc.

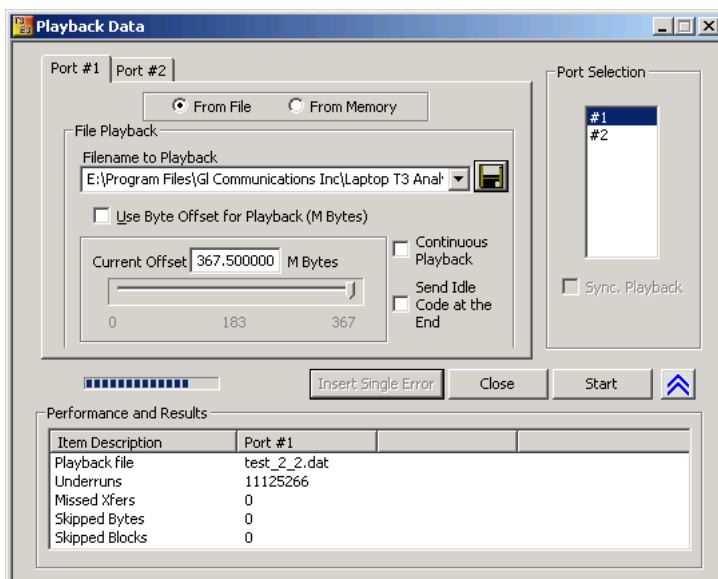
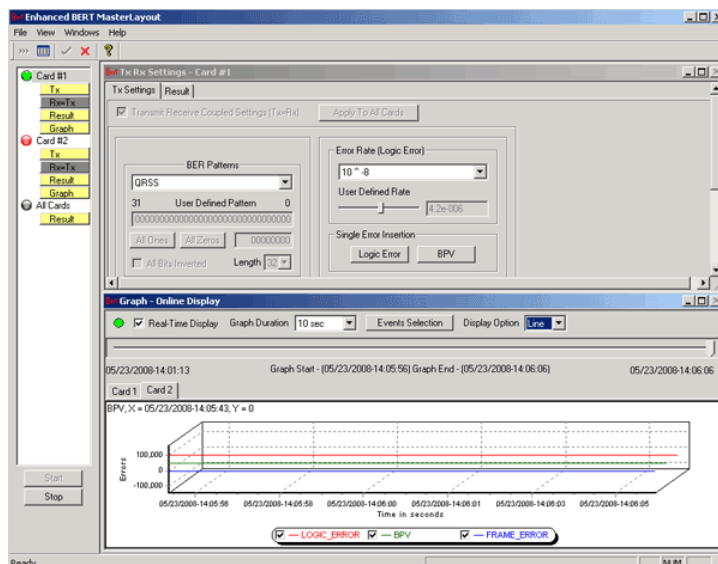
818 West Diamond Avenue - Third Floor. Gaithersburg, MD 20878 • (V) 301-670-4784 (F) 301-670-9187

Web Page Address: <http://www.gl.com/> • E-Mail Address: gl-info@gl.com

Applications

BERT (Full Frame and Unframed)

- Test Patterns:
 - PRBS:QRSS, 26-1, 29-1, 211-1, 215-1, 220-1, 223-1
 - Static: All 1s, All 0s, 1010, 1 in 7, 3 in 24., CSU Loop-Up, CSU Loop-Down, NIU Loop-Up, NIU Loop-Down
 - User Defined: 1 bits to 32-bits
- Performance Analysis: ITU-T G.82, G.826, M.2100, M.2110, M.2120
- Bit Error Insertion: Single Manual error, Automated error rate 10^{-2} through 10^{-9} , User defined error rate
- Logging
- Graphical Display

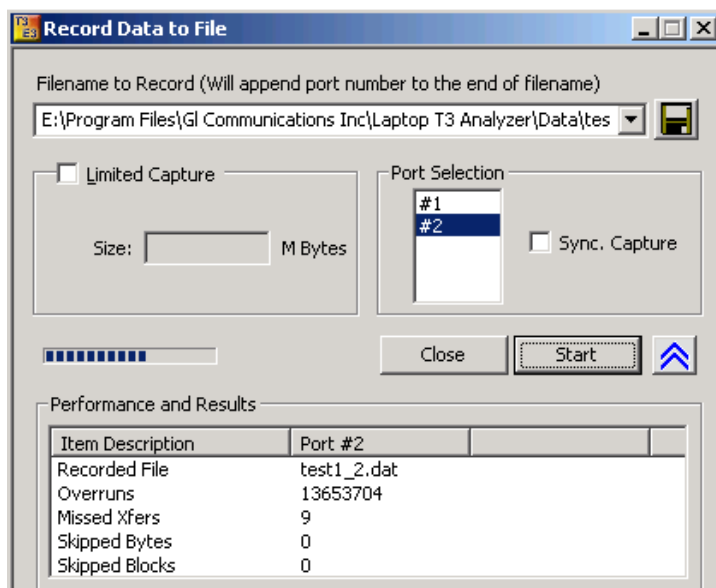


Playback Data (Raw file)

- Playback flat binary file over T3/E3
- User selected file without any size constraints
- Playback over framed or unframed T3/E3
- Option for continuous playback or single shot
- Allows manual insertion of bit error

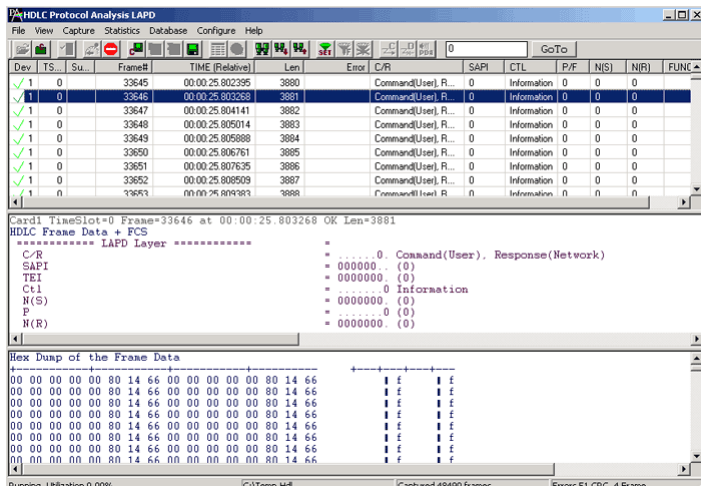
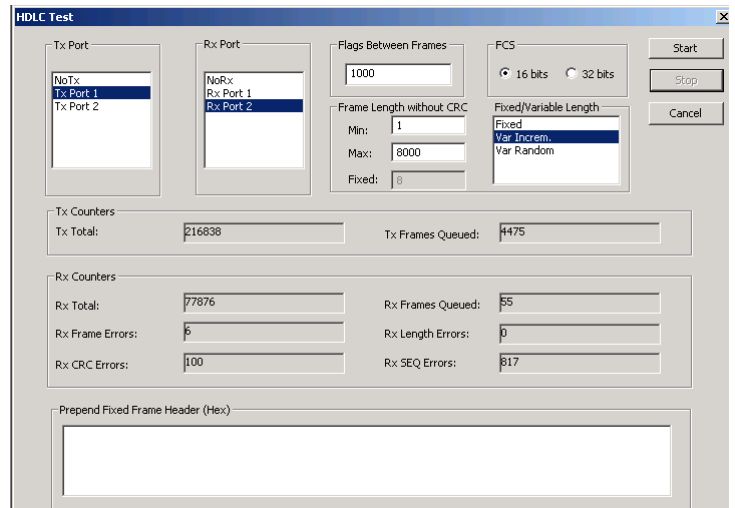
Record Data to File (Raw)

- Capture incoming data into binary flat File
- Each T3/E3 Signal is captured into separate files
- Synchronized capture from both ports
- Unframed T3/E3 or Framed T3/E3
- Capture up to user selected size or manually stop



HDLC Tx/Rx Test

- Transmit HDLC at wire speed
 - Generate HDLC frames of varying length
 - HDLC frames contain sequence numbers
 - User controllable flags in between frames
 - User selectable HDLC frame size
 - Option for CRC16 or CRC32 bits
 - Allows pre-pending user-defined frame header for each HDLC frame, which allows to create PPP, Frame-relay simulation
- Receive and analyze HDLC at wire speed
 - Verify received HDLC frames for integrity
 - Analyzer receives frames and counts CRC errors, frame errors, length error and sequence errors



Protocol Analyzers

- HDLC Protocol Analyzer
 - Analyze HDLC over bidirectional T3/E3
 - All the capabilities as we have in T1/E1 analyzer
- Frame Relay Protocol Analyzer
 - Analyze Frame Relay over bidirectional T3/E3
 - All the capabilities as we have in T1/E1 analyzer
- PPP Protocol Analyzer
 - Analyze PPP over bidirectional T3/E3
 - All the capabilities as we have in T1/E1 analyzer
- ATM Protocol Analyzer
 - Analyze Direct-Mapped ATM over bidirectional T3 (E3 is coming soon)
 - All the capabilities as we have in T1/E1 analyzer

Coming soon

- Inline Error Insertion and Delay Simulation
- ATM BERT Testing



Specifications (USB T1E1 units, HD T1E1 Cards)

Connectors

T3/E3: BNC (2 Tx, 2 Rx)
T1/E1: RJ-45 (2 Tx, 2 Rx) for Drop/Insert
External Clock: MBX (2)
PC Interface: USB 2.0
External Power: 9 VDC

T3/E3 Line Interface

Output Amplitude: 800mV +/- 50mV
Input Impedance: 75 Ohms unbalanced (BNC)
Line Code: B3ZS (T3), HDB3 (E3)
Terminate Input Level: 0.09Vp – 0.85Vp
Monitor Input Level: 0.025Vp – 0.08Vp
Clock Source:
Internal +/- 1 PPM @25C [+/- 4.5 ppm (includes ageing, stability)]
Recovered Clock recovered from receiver
External TTL Level signal

- **High Speed:** (T3/E3 Rate)
- **Low Speed:** (2KHz, 8KHz, 2MHz, 1.5MHz)Recovered from Inserted T1 or E1

T3/E3 Transmitter

T3/E3 Payloads: Framed T3/E3 Data, Unframed T3/E3, Idle, AIS
T3 Framing Modes:
Unframed,
M13 (ANSI T1-107 – 1995) - Structured (Channelized), and Unstructured (Unchannelized)
C-bit (ANSI T1-107 – 1990) - Structured (Channelized), and Unstructured (Unchannelized)
E3 Framing Modes:
Unframed,
E13 (for E3) - Structured (Channelized), and Unstructured (Unchannelized)
Framed T3/E3 Unstructured Payload:
Raw Data from File, ATM Cells (only for T3), HDLC Frames, BERT Patterns
Unframed E3 Payload: Raw Data from File, BERT Patterns
Channel Structure: T1, E1 (ITU-T G.747)
BERT Patterns: QRSS, 2⁶-1, 2⁹-1, 2¹¹-1, 2¹⁵-1, 2²⁰-1, 2²³-1, User Defined up to 32-bits, other static patterns
T1 Payload: Inserted T1, AIS, Loopback, BERT Patterns
E1 Payload: Inserted E1, AIS, Loopback, BERT Patterns
Loopbacks: Complete T3/E3 Signal, Selected T1s/E1s from incoming T3/E3

T3/E3 Receiver

T3 Framing Format:
M13 (ANSI T1-107 – 1995), C-bit (ANSI T1-107 – 1990), Unframed, Structured (Channelized), and Unstructured (Unchannelized)
E3 Framing Format:
E13, Unframed, Structured(Channelized), and Unstructured (Unchannelized)
Channel Structure: T1/E1 (ITU-T G.747)
Framed T3/E3 Unstructured Payload:
Raw Data Captured to File, ATM Analysis (only for T3), HDLC Frames Analysis, BERT Patterns Measurement
Framed T3/E3 Structured Payload:
Raw Data Captured to File, BERT Patterns Measurement, Drop Selected T1(s) / E1(s)

Transmit

T3/E3 Line Rate Offset: +/- 50 PPM in 1 ppm Steps
Level Measurement: Supported
T3 Error Add:
Payload Bit, FAS, MFAS, FAS+MFAS, BPV, C-bit, P-bit, FEBE, EXZ (for T3)
E3 Error Add:
Payload Bit, Frame Errors, Code Violation (CV) Error, EXZ, FAS
T3 Alarm Generation: LOS, OOF, AIS, RAI (X-bit), Idle, FEAC Codes (Loopback and alarm/status codes)
E3 Alarm Generation: LOS, OOF, RAI (X-bit);
E3 Alarm Monitoring: LOS, LOF, AIS, RAI (X-bit), EXZ
T3 FEAC Codes: Alarm status codes, loopback codes with channel indicator for T1

Buyers Guide:

[TE3001](#) - Portable (USB) Dual T3 E3 / T1 E1 Hardware Unit - requires TT3001 or EE3001
[TT3001 / EE3001](#) - w/ Analyzer Basic Software for WIN XP/Vista
[TT3020 / EE3020](#) - Record Playback Software
[TT3090 / EE3090](#) - HDLC Tx/Rx Test + Analyzer
[TT3135 / EE3135](#) - Analysis & decode of ML-PPP & PPP over T3
[TT3130 / EE3130](#) - Analysis and decode of Frame Relay over T3

Related Hardware

[UT301 / UT302](#) - T3 Analysis PCI Card w/ Basic Software and Client / Server and Command Line Utility
*Specifications are subjected to change

